**Assignment 3**

All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

Copy-paste or type the unique URL of your assignment solution from website [www.edaplayground.com](http://www.edaplayground.com) for assignment questions. Please note that do not copy someone else’s link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

**Q1:** Implement a NOT gate using one 2-input NAND gate only. Write its verilog code also.

**Ans: Link1:** [**https://www.edaplayground.com/x/qzq8**](https://www.edaplayground.com/x/qzq8)

**Q2:** Write Verilog code and testbench using data flow modeling for Y = ABC + AB +AC.

**Ans: Link2:** [**https://www.edaplayground.com/x/gQSP**](https://www.edaplayground.com/x/gQSP)

**Q3:** Write Verilog code and testbench using structural modeling for Y = (A+B+C).(A+B).(A+C)

**Ans: Link3: https://edaplayground.com/x/96H\_**

**Q4:** Write Verilog code and testbench for detecting even parity error in 4 bit (3+1) binary number.

**Ans: Link4: https://www.edaplayground.com/x/GAn\_**